**Pinout Chart for the DE2 Evaluation Board**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Signal Name** | **FPGA Pin No.** | **Signal Name** | **FPGA Pin No.** | **Signal Name** | **FPGA Pin No.** |
| SW[0] | PIN\_N25 | HEX2[e] | PIN\_AB26 | LEDR[0] | PIN\_AE23 |
| SW[1] | PIN\_N26 | HEX2[f] | PIN\_AB25 | LEDR[1] | PIN\_AF23 |
| SW[2] | PIN\_P25 | HEX2[g] | PIN\_Y24 | LEDR[2] | PIN\_AB21 |
| SW[3] | PIN\_AE14 | HEX3[a] | PIN\_Y23 | LEDR[3] | PIN\_AC22 |
| SW[4] | PIN\_AF14 | HEX3[b] | PIN\_AA25 | LEDR[4] | PIN\_AD22 |
| SW[5] | PIN\_AD13 | HEX3[c] | PIN\_AA26 | LEDR[5] | PIN\_AD23 |
| SW[6] | PIN\_AC13 | HEX3[d] | PIN\_Y26 | LEDR[6] | PIN\_AD21 |
| SW[7] | PIN\_C13 | HEX3[e] | PIN\_Y25 | LEDR[7] | PIN\_AC21 |
| SW[8] | PIN\_B13 | HEX3[f] | PIN\_U22 | LEDR[8] | PIN\_AA14 |
| SW[9] | PIN\_A13 | HEX3[g] | PIN\_W24 | LEDR[9] | PIN\_Y13 |
| SW[10] | PIN\_N1 | HEX4[a] | PIN\_U9 | LEDR[10] | PIN\_AA13 |
| SW[11] | PIN\_P1 | HEX4[b] | PIN\_U1 | LEDR[11] | PIN\_AC14 |
| SW[12] | PIN\_P2 | HEX4[c] | PIN\_U2 | LEDR[12] | PIN\_AD15 |
| SW[13] | PIN\_T7 | HEX4[d] | PIN\_T4 | LEDR[13] | PIN\_AE15 |
| SW[14] | PIN\_U3 | HEX4[e] | PIN\_R7 | LEDR[14] | PIN\_AF13 |
| SW[15] | PIN\_U4 | HEX4[f] | PIN\_R6 | LEDR[15] | PIN\_AE13 |
| SW[16] | PIN\_V1 | HEX4[g] | PIN\_T3 | LEDR[16] | PIN\_AE12 |
| SW[17] | PIN\_V2 | HEX5[a] | PIN\_T2 | LEDR[17] | PIN\_AD12 |
|  |  | HEX5[b] | PIN\_P6 |  |  |
| KEY[0] | PIN\_G26 | HEX5[c] | PIN\_P7 | LEDG[0] | PIN\_AE22 |
| KEY[1] | PIN\_N23 | HEX5[d] | PIN\_T9 | LEDG[1] | PIN\_AF22 |
| KEY[2] | PIN\_P23 | HEX5[e] | PIN\_R5 | LEDG[2] | PIN\_W19 |
| KEY[3] | PIN\_W26 | HEX5[f] | PIN\_R4 | LEDG[3] | PIN\_V18 |
|  |  | HEX5[g] | PIN\_R3 | LEDG[4] | PIN\_U18 |
| HEX0[a] | PIN\_AF10 | HEX6[a] | PIN\_R2 | LEDG[5] | PIN\_U17 |
| HEX0[b] | PIN\_AB12 | HEX6[b] | PIN\_P4 | LEDG[6] | PIN\_AA20 |
| HEX0[c] | PIN\_AC12 | HEX6[c] | PIN\_P3 | LEDG[7] | PIN\_Y18 |
| HEX0[d] | PIN\_AD11 | HEX6[d] | PIN\_M2 | LEDG[8] | PIN\_Y12 |
| HEX0[e] | PIN\_AE11 | HEX6[e] | PIN\_M3 |  |  |
| HEX0[f] | PIN\_V14 | HEX6[f] | PIN\_M5 | LCD\_D[0] | PIN\_J1 |
| HEX0[g] | PIN\_V13 | HEX6[g] | PIN\_M4 | LCD\_D[1] | PIN\_J2 |
| HEX1[a] | PIN\_V20 | HEX7[a] | PIN\_L3 | LCD\_D[2] | PIN\_H1 |
| HEX1[b] | PIN\_V21 | HEX7[b] | PIN\_L2 | LCD\_D[3] | PIN\_H2 |
| HEX1[c] | PIN\_W21 | HEX7[c] | PIN\_L9 | LCD\_D[4] | PIN\_J4 |
| HEX1[d] | PIN\_Y22 | HEX7[d] | PIN\_L6 | LCD\_D[5] | PIN\_J3 |
| HEX1[e] | PIN\_AA24 | HEX7[e] | PIN\_L7 | LCD\_D[6] | PIN\_H4 |
| HEX1[f] | PIN\_AA23 | HEX7[f] | PIN\_P9 | LCD\_D[7] | PIN\_H3 |
| HEX1[g] | PIN\_AB24 | HEX7[g] | PIN\_N9 | LCD\_RW | PIN\_K4 |
| HEX2[a] | PIN\_AB23 |  |  | LCD\_EN | PIN\_K3 |
| HEX2[b] | PIN\_V22 | UART\_RX | PIN\_C25 | LCD\_RS | PIN\_K1 |
| HEX2[c] | PIN\_AC25 | UART\_TX | PIN\_B25 | LCD\_ON | PIN\_L4 |
| HEX2[d] | PIN\_AC26 |  |  | LCD\_BL | PIN\_K2 |

**Pinout Chart for the DE2 Evaluation Board (continued)**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Signal Name** | **FPGA Pin No.** | **Signal Name** | **FPGA Pin No.** | **Signal Name** | **FPGA Pin No.** |
| VGARed[0] | PIN\_C8 | VGAGrn[8] | PIN\_E12 | ADC clk | PIN\_C5 |
| VGARed[1] | PIN\_F10 | VGAGrn[9] | PIN\_D12 | ADC data | PIN\_B5 |
| VGARed[2] | PIN\_G10 | VGABlu[0] | PIN\_J13 | DAC clk | PIN\_C6 |
| VGARed[3] | PIN\_D9 | VGABlu[1] | PIN\_J14 | DAC data | PIN\_A4 |
| VGARed[4] | PIN\_C9 | VGABlu[2] | PIN\_F12 | Chip clk | PIN\_A5 |
| VGARed[5] | PIN\_A8 | VGABlu[3] | PIN\_G12 | Bit-strm clk | PIN\_B4 |
| VGARed[6] | PIN\_H11 | VGABlu[4] | PIN\_J10 | I2C data | PIN\_A6 |
| VGARed[7] | PIN\_H12 | VGABlu[5] | PIN\_J11 | I2C clk | PIN\_B6 |
| VGARed[8] | PIN\_F11 | VGABlu[6] | PIN\_C11 |  |  |
| VGARed[9] | PIN\_E10 | VGABlu[7] | PIN\_B11 | PS/2 clk | PIN\_D26 |
| VGAGrn[0] | PIN\_B9 | VGABlu[8] | PIN\_C12 | PS/2 data | PIN\_C24 |
| VGAGrn[1] | PIN\_A9 | VGABlu[9] | PIN\_B12 |  |  |
| VGAGrn[2] | PIN\_C10 |  |  | IRDA Trans | PIN\_AE24 |
| VGAGrn[3] | PIN\_D10 | VGA clock | PIN\_B8 | IRDA Rec | PIN\_AE25 |
| VGAGrn[4] | PIN\_B10 | VGA blank | PIN\_D6 |  |  |
| VGAGrn[5] | PIN\_A10 | VGAHsync | PIN\_A7 | 27MHz Clk | PIN\_D13 |
| VGAGrn[6] | PIN\_G11 | VGAVsync | PIN\_D8 | 50MHz Clk | PIN\_N2 |
| VGAGrn[7] | PIN\_D11 | VGAsync | PIN\_B7 | Ext Clk | PIN\_P26 |

**Pinout Chart for 40 Pin Header**

**(looking down at breadboard)**

|  |  |  |
| --- | --- | --- |
| PIN\_D25 | 1 | PIN\_J22 |
| PIN\_E26 | 2 | PIN\_E25 |
| PIN\_F24 | 3 | PIN\_F23 |
| PIN\_J21 | 4 | PIN\_J20 |
| PIN\_F25 | 5 | PIN\_F26 |
| +5V | 6 | GND |
| PIN\_N18 | 7 | PIN\_P18 |
| PIN\_G23 | 8 | PIN\_G24 |
| PIN\_K22 | 9 | PIN\_G25 |
| PIN\_H23 | 10 | PIN\_H24 |
| PIN\_J23 | 11 | PIN\_J24 |
| PIN\_H25 | 12 | PIN\_H26 |
| PIN\_H19 | 13 | PIN\_K18 |
| PIN\_K19 | 14 | PIN\_K21 |
| +3.3V | 15 | GND |
| PIN\_K23 | 16 | PIN\_K24 |
| PIN\_L21 | 17 | PIN\_L20 |
| PIN\_J25 | 18 | PIN\_J26 |
| PIN\_L23 | 19 | PIN\_L24 |
| PIN\_L25 | 20 | PIN\_L19 |